



POWER CONSUMPTION BENCHMARKING FOR RECONFIGURABLE PLATFORMS

Teemu Pitkänen

Peter Jamieson

Tobias Becker

Sami Moisio

Jarmo Takala

Tampere University of Technology, Finland

Miami University , Oxford, UT, USA

Imperial College, London, UK

Nokia, Tampere, Finland

Tampere University of Technology, Finland



TAMPERE UNIVERSITY OF TECHNOLOGY

Imperial College
London



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Outline

GroundHog 2009 benchmark suite
Power measurement system
Experiments



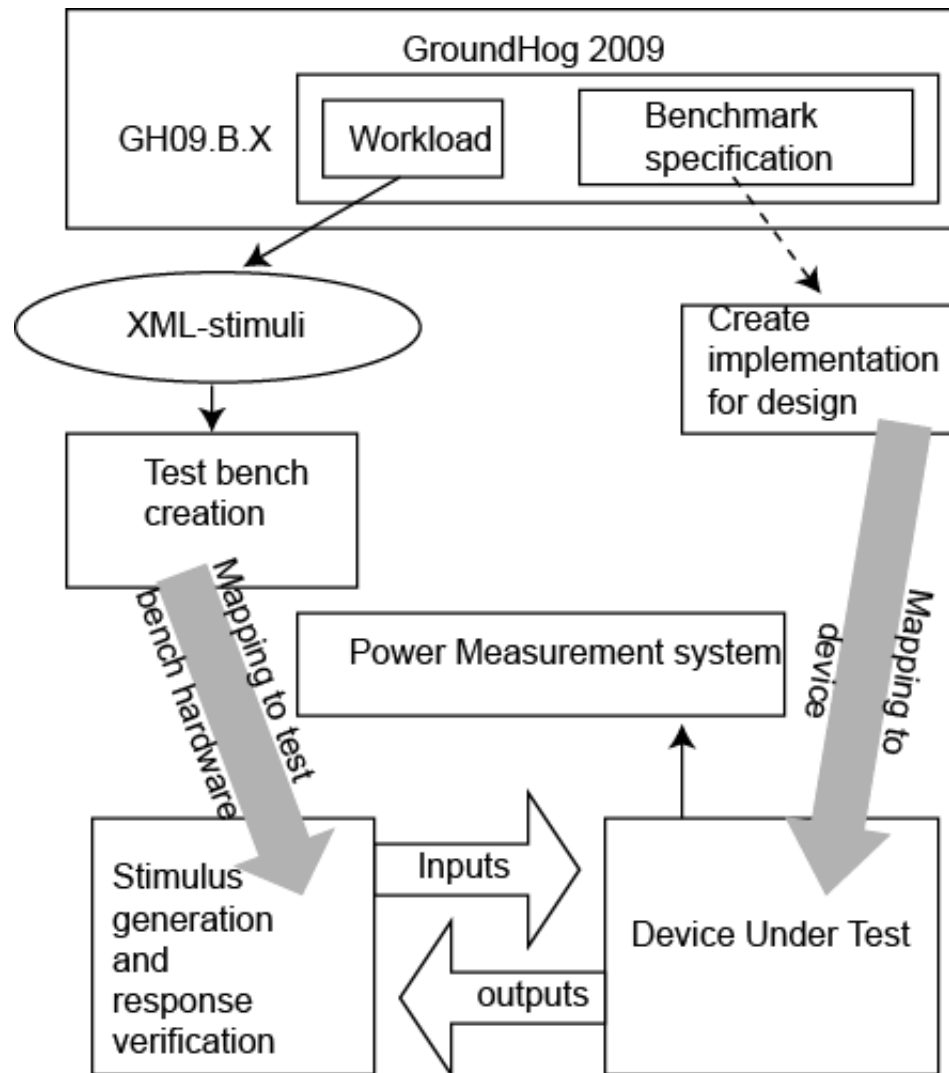


GroundHog 2009 – benchmark suite

- Open source benchmark suite for reconfigurable architectures in mobile domain
 - High level benchmark
 - Includes 7 benchmark cases
 - Golden simulation model
 - Textual specification of the design
 - Includes stimulus specifications



GroundHog 2009 – Principle



GroundHog 2009 – Benchmark cases

GH09.B.0 - Fabric analysis

GH09.B.1 - Port Expander and Keypad Controller

GH09.B.2 - Glue Logic

GH09.B.3 - Cryptography

GH09.B.4 - Data Compression

GH09.B.5 - Bridge Chip

GH09.B.6 - 2D convolution

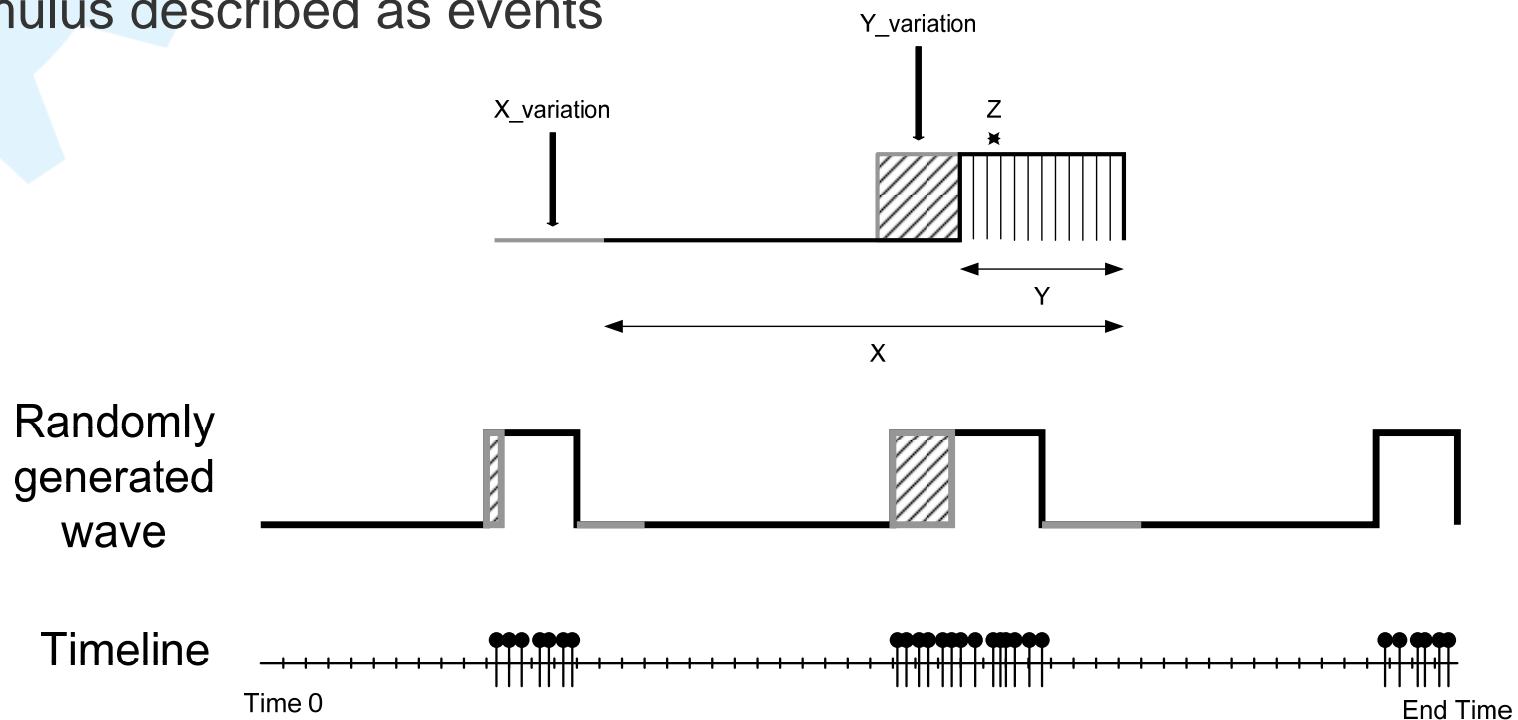


GroundHog 2009 – Stimulus definition for benchmark designs

Workload - Timeline of stimuli

- Each design has dedicated parameter set which defines stimuli
- Parameters can be set by user

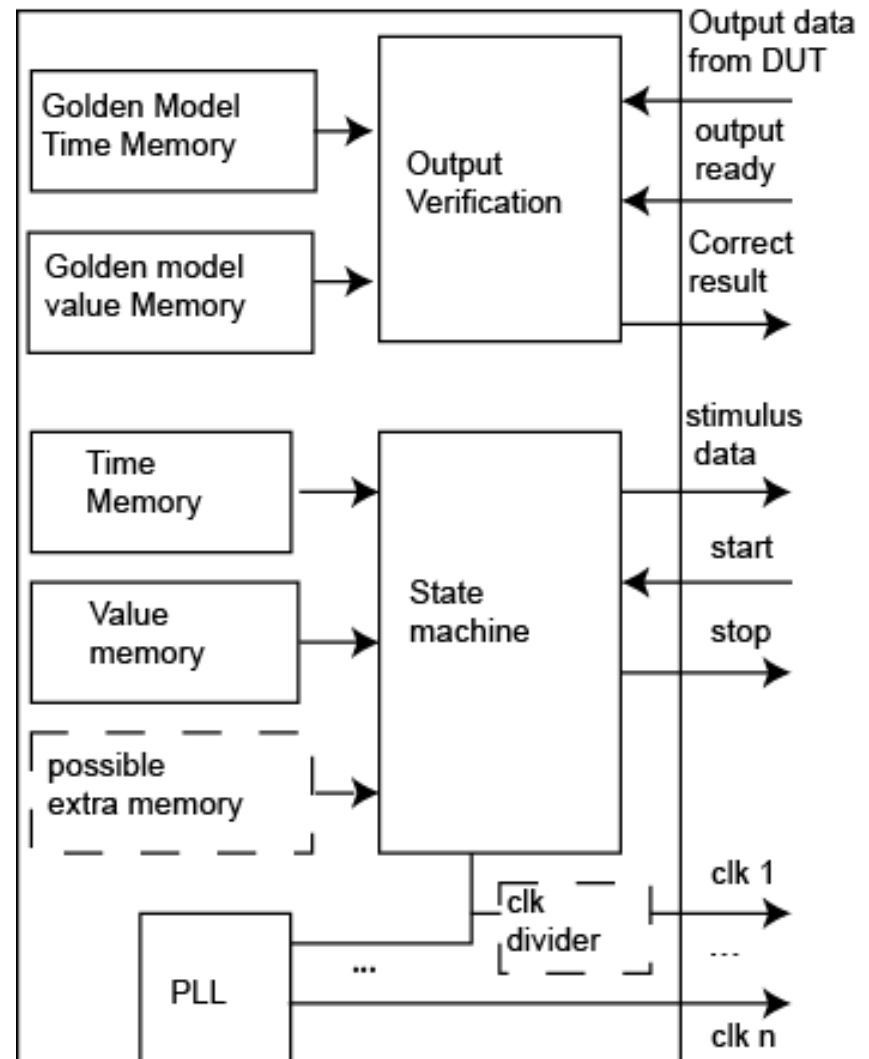
Stimulus described as events





RTL – Testbench

- Groundhog stimulus defined as events
 - action and time for the action
- We have developed testbench generator
 - Parses GroundHog stimulus files
 - Generates VHDL testbench realizing the defined stimulus
 - Creates test vectors for the response from the golden model



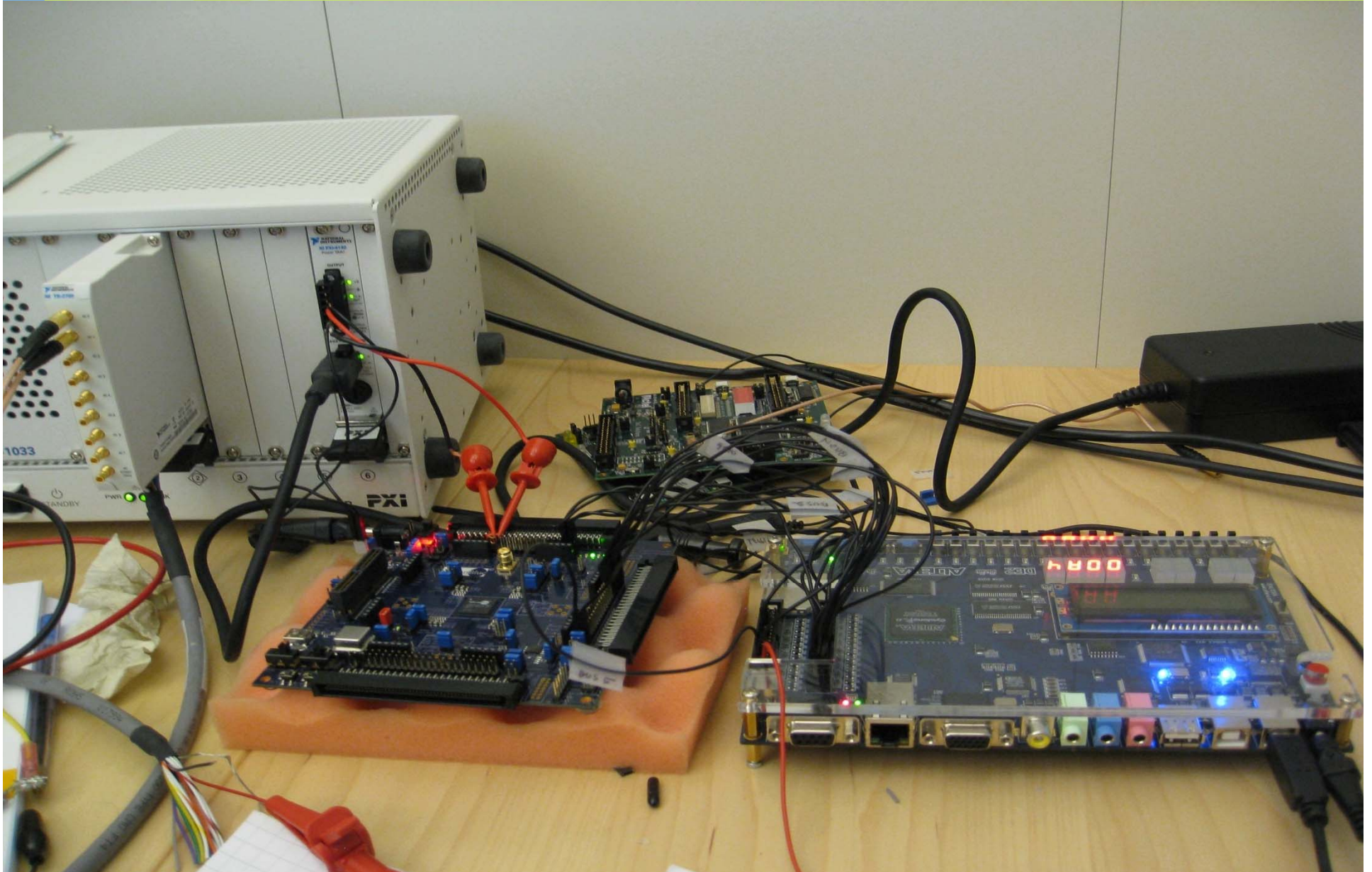
Experiments

We have analysed power consumption of the following devices

DEVICE	Resources	Memory [bits]
AGL600	13824 LUTs flash 130nm	108k
iCE65LO4	3520 LUTs, SRAM 65nm	80k
iCE65LO4-i	Improved version of 65L04	
iCE65LO8	Higher capacity version of iCE65L04; 7680 LUTs, SRAM 65 nm	128k
XO2-1200	1280 LUTs, SRAM 65nm	64k
PSOC3	8051 + configurable blocks	64k



Experiments



Experiments

	expander	Glue logic	AES	LZW	P/S	2D Convolution
AGL600	3.5 [10%]	1.1 [1%]	20 ⁽¹⁾ [86%]	9.2 [1 / 100 %]	1.8 [1%]	5.9 [19 / 40 %]
iCE65LO4	1.8 [28%]	1.7 [4%]				
iCE65LO4-i			13 [47%]	0.6 [10 / 80 %]	0.5 [3%]	0.6 [23 / 45 %]
iCE65LO8	-	-		1.2 [7 / 100 %]		1.1 [11 / 28 %]
XO2-1200	1.2 [63%]	1.2 [62%]		0.5 [17 / 86%]	0.3 [5%]	1.1 [59 / 57 %]
PSOC3	-		63 ⁽¹⁾			

[resource utilization / {memory utilization}]

All designs 1.2V V_{DD}

(1) AGL600 1.5V V_{DD} @10 MHz, PSOC3 @32MHz



Experiments

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AGL600	3.5 [10%]	1.1 [1%]	20 [86%]	9.2 [1 / 100%]	1.8 [1%]	5.9 [19 / 40%]
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PSOC3	-		62			

- AGL600: High memory power consumption, slow memories
- iCE65LO4: clock tree consumes power (roughly 1.5 mW)
- iCE65LO8: larger number of resources consumes more power
- XO2: poor synthesis tools
 - Multiplication consumes power
 - Expander and glue logic use the same amount of resources
- PSOC3: requires 3x clock frequency



How to reduce power dissipation: Clock manipulation

- With XO2-1200 we have done
 - Clock tree is manipulated with on-chip clock enables

Design	P_{AVG} [mW]	Improvement [%]
B.1	0.14	~750
B.4	0.28	~60
B.5	0.09	~240
B.6	0.08	~1100

- On-chip clock muxes allows use of several external clocks

Design	P_{AVG} [mW]	Improvement [%]
B.2	0.58	~40



Other observations

- PLL consumes power
 - AGL600: PLL consumes ~1.5 mW
- Sleep modes saves power
 - AGL600: flash freeze mode
 - 46 μ W (benchmarks required at least 1 mW)
 - wake up latency restricts usage
- Power dissipation increase at higher temperature
- Larger chip consumes more power



Conclusion

- Testbench architecture for GroundHog 2009
- Designer choices affects the power dissipation
- GroundHog benchmark suite including tools
<http://cc.doc.ic.ac.uk/projects/GROUNDHOG/>
- Power measurement testbenches and reference implementations
<http://www.cs.tut.fi/projects/GroundHog2009/>
- Repository for community designs
http://opencores.org/project,groundhog2009_repository,overview

